IN THE CLAIMS

1 (Currently Amended). A method comprising:

monitoring ~~the~~ a temperature of a cache memory; and

in response to a detection of a temperature condition, transitioning the cache memory from a write-back cache to a write-through cache.

2 (Original). The method of claim 1 including monitoring the temperature of a ferroelectric polymer cache memory.

3 (Original). The method of claim 1 including adjusting the operation of a system using said memory at a first temperature and, in response to the detection of a higher, second temperature, transitioning the cache from a write-back cache to a write-through cache.

4 (Original). The method of claim 3, including slowing an operation of said system at said first temperature.

5 (Original). The method of claim 3 including reducing pre-fetching at said first temperature.

6 (Original). The method of claim 3 including adjusting what data is cached based on the detection of said first temperature.

7 (Original). The method of claim 3 including shutting off the said cache memory at a temperature above said second temperature.

8 (Original). The method of claim 7 including monitoring for a temperature lower than said second temperature.

9 (Original). The method of claim 8 including, upon detecting a lower temperature, resuming operation of said cache memory.

10 (Original). The method of claim 8 including waiting for a power cycle before resuming cache operations.

11 (Original). The method of claim 7 including shutting off said cache memory and invalidating cache lines in said cache memory.

12 (Original). The method of claim 1 including flushing a cache line in said cache memory that has not been written through to a source memory.

13 (Currently Amended). An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

monitor ~~the~~ a temperature of a cache memory; and

in response to the detection of a temperature condition, transition the cache memory from a write-back cache to a write-through cache memory.

14 (Original). The article of claim 13 further storing instructions that, if executed, enable a processor-based system to monitor the temperature of a ferroelectric polymer cache memory.

15 (Original). The article of claim 13 further storing instructions that, if executed, enable a processor-based system to adjust the operation of a system using said memory at a first temperature and, in response to the detection of a higher, second temperature, transition the cache memory from a write-back to a write-through cache.

16 (Original). The article of claim 13 further storing instructions that, if executed, enable a processor-based system to shut off the said cache memory at a temperature above said second temperature.

17 (Original). The article of claim 13 further storing instructions that, if executed, enable a processor-based system to flush a cache line in said cache memory that has not been written through to a source memory.

18 (Original). The article of claim 17 further storing instructions that, if executed, enable a processor-based system to monitor for a temperature lower than said second temperature.

19 (Original). The article of claim 18 further storing instructions that, if executed, enable a processor-based system to resume operation of said cache memory upon detecting a lower temperature.

20 (Original). The article of claim 18 further storing instructions that, if executed, enable a processor-based system to wait for a power cycle before resuming cache operations.

21 (Original). The article of claim 16 further storing instructions that, if executed, enable a processor-based system to shut off the cache and invalidate all the cache lines.

22 (Original). The article of claim 13 further storing instructions that, if executed, enable a processor-based system to transition the cache memory from a write-back to cache to a write-through cache memory at a first, higher temperature and to adjust for the slower speed of the cache memory at a second temperature lower than said first temperature.

23 (Original). The article of claim 22 further storing instructions that, if executed, enable a processor-based system to reduce the speed of operations at said second temperature.

24 (Original). The article of claim 22 further storing instructions that, if executed, enable a processor-based system to reduce pre-fetching at said second temperature.

25 (Original). The article of claim 22 further storing instructions that, if executed, enable a processor-based system to adjust the caching of data based on the detection of said second temperature.

26 (Currently Amended). A processor-based system comprising:

a processor;

a disk drive coupled to said processor;

a cache memory coupled said processor; and

a storage to store a cache driver to monitor ~~the~~ a temperature of said cache memory and in response to the detection of a temperature condition, transition the cache memory from a write-back cache memory to a write-through cache memory.

27 (Original). The system of claim 26 wherein said cache memory is a ferroelectric polymer cache memory.

28 (Original). The system of claim 26 wherein said cache memory is a flash memory.

29 (Original). The system of claim 26 wherein said storage stores instructions that enable dirty lines to be flushed.

30 (Original). The system of claim 26 wherein said storage stores instructions that enable the system to adjust for reduced speed operation at a first temperature, switch to a write-through cache memory at a second higher temperature, and invalidate cache lines and shut off the cache memory at still a higher temperature.

31 (Original). The system of claim 30, said storage further storing instructions that enable the cache memory to return to full speed operation.

32 (Original). The system of claim 30 wherein said storage stores instructions that enable the system to wait for reduced speed temperature range to resume cache operations after shutting off the cache memory in response to a temperature condition.

33 (Original). The system of claim 30 wherein said storage stores instructions that enable the system to resume cache operations after shutting off the cache memory in response to a cache condition by initially resuming reduced speed operations in a first stage and thereafter resuming normal operations.

34 (Original). The system of claim 26 wherein said cache memory includes a temperature sensor.

35 (Currently Amended). A circuit comprising:

a component to receive an indication of ~~the~~ a temperature of a cache memory and to develop a signal to transition the cache memory from a write-back cache to a write-through cache in response to said temperature indication.

36 (Original). The circuit of claim 35 wherein said component to vary the operation of a system to adjust for the temperature affected operation of said cache memory.

37 (Original). The circuit of claim 36 wherein said component to adjust a caching operation of the system in response to a temperature indication from said memory.

38 (Original). The circuit of claim 36 wherein said component to shut off said cache in response to a temperature indication.

39 (Original). The circuit of claim 38 wherein said component to invalidate a cache line in said cache memory.

40 (Original). The circuit of claim 35 including a cache memory.

41 (Original). The circuit of claim 40 including a ferroelectric polymer memory.

42 (Original). The circuit of claim 40 wherein said cache memory includes a temperature sensor.

Claims 43-45 (Canceled).

46 (Previously Presented). A method comprising:

monitoring a temperature; and

in response to a detection of a temperature condition, operating a cache memory in one of two different modes depending on the temperature.

47 (Previously Presented). The method of claim 46 including monitoring the temperature of a ferroelectric polymer cache memory.

48 (Previously Presented). The method of claim 46 including adjusting the operation of a system using said memory at a first temperature and, in response to the detection of a higher, second temperature, transitioning the cache from a write-back cache to a write-through cache.

49 (Previously Presented). The method of claim 48, including slowing an operation of said system at said first temperature.

50 (Previously Presented). The method of claim 48 including reducing pre-fetching at said first temperature.

51 (Previously Presented). A computer readable medium storing instructions that, if executed, enable a processor-based system to:

monitor a temperature of a cache memory; and

in response to the detection of a temperature condition, operating a cache memory in one of two different modes depending on the temperature.

52 (Previously Presented). The medium of claim 51 further storing instructions that, if executed, enable a processor-based system to monitor the temperature of a ferroelectric polymer cache memory.

53 (Previously Presented). The medium of claim 51 further storing instructions that, if executed, enable a processor-based system to adjust the operation of a system using said memory

at a first temperature and, in response to the detection of a higher, second temperature, transition the cache memory from a write-back to a write-through cache.

54 (Previously Presented). A circuit comprising:

a cache memory; and

a component to receive an indication of a temperature and to develop a signal to transition the cache memory from a first to a second operating mode in response to said temperature indication.

55 (Previously Presented). The circuit of claim 54 wherein said component to vary the operation of a system to adjust for the temperature affected operation of said cache memory.

56 (Previously Presented). The circuit of claim 55 wherein said component to adjust a caching operation of the system in response to a temperature indication from said memory.

57 (Previously Presented). The circuit of claim 55 wherein said component to shut off said cache in response to a temperature indication.

58 (Previously Presented). The circuit of claim 57 wherein said component to invalidate a cache line in said cache memory.

59 (Previously Presented). The circuit of claim 54 including a ferroelectric polymer memory.